CONTACT INFORMATION

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EDUCATION

- **M.S. CHEMICAL ENGINEERING, OREGON STATE UNIVERSITY, 2015**
- **B.S. CHEMICAL ENGINEERING, UNIVERSITY OF WASHINGTON, 2013**

KEY SKILLS

- **Wet etch and thin film deposition unit process ownership**
- **Statistical process control and capability analysis**
- **Designed experiments (full factorial, response surface)**
- **Copy-exact and tool matching**
- **Equipment qualification protocols**
- **Wafer defect and yield analysis**
- **Recipe development and PM tuning**
- **Python and structured query languages for tool data**
- **8D and Kepner-Tregoe root cause analysis**
- **Cross-fab technology transfer**

ELENA VASQUEZ

Process Engineer

Senior process engineer with nine years across semiconductor wet etch and thin film deposition modules. Leads yield and capability work end to end, from statistical control setup and designed experiments through equipment qualification and copy-exact transfers between fabs. Known for pulling clean signal out of noisy tool data.

PROFESSIONAL EXPERIENCE

SENIOR PROCESS ENGINEER, WET ETCH | CASCADIA SILICON WORKS, PORTLAND, OR | 2020 - PRESENT

- Own three wet etch modules covering roughly 45% of front-end wafer starts, with defect density held under the tool target for seven of the last eight quarters.
- Led the qualification of a new SC-1 chemistry that dropped particle adds per wafer from 42 to 11 while keeping etch rate within 2% of the incumbent bath.
- Ran the copy-exact transfer of two recipes to the sister fab in Arizona, including 30 matching runs and the joint capability report.
- Set up statistical process control charts for critical dimension bias and trained six engineers on out-of-control action plans.
- Chaired the weekly module review with equipment, integration, and yield, driving the top-five excursion list to closure.

PROCESS ENGINEER, THIN FILM DEPOSITION | AUREON MICROELECTRONICS, HILLSBORO, OR | 2017 - 2020

- Qualified two plasma-enhanced deposition tools for a new nitride film, including thickness uniformity and stress mapping across 25 sites per wafer.
- Investigated an intermittent flake defect and traced it to chamber season count, closing with a revised PM trigger that cut the excursion rate roughly in half.
- Wrote the process spec and control plan for a low-k dielectric transferred from development.
- Mentored two junior engineers through their first tool qualifications.

PROCESS ENGINEER | AUREON MICROELECTRONICS, HILLSBORO, OR | 2015 - 2017

- Supported day-to-day operations on four etch tools, including recipe edits, tool matching, and PM sign-offs.
- Reduced rework on a critical implant step through a designed experiment on post-etch clean parameters.
- Rotated through the yield group for one quarter and contributed to a wafer-map signature library.