



Siddharth Kamara

Senior Hardware Engineer

Hardware engineer with 6 years of experience in FPGA design, board-level verification, and signal integrity analysis, achieving a 96.7% hardware validation pass rate by standardizing simulation and board-level test sequences and reviewing interface specifications with design staff. Reduced security vulnerabilities by 29.3% on a network gateway module by applying cybersecurity system hardening requirements and patching firmware-level exploits. Skilled in VHDL, Python, MATLAB, and network analyzers across mixed-signal and digital platforms.

CONTACT INFORMATION

 (802) 555-0125
 siddharth.kamara@example.com
 Brattleboro, VT 12345

EDUCATION

BS Electrical Engineering
University of Vermont, Burlington, VT
2016 – 2020

KEY SKILLS

- VHDL
- FPGA Design
- Python
- MATLAB
- Digital Oscilloscopes
- Network Analyzers
- Signal Integrity Analysis
- Cybersecurity System Hardening
- Design Verification Testing
- Schematic Review
- Board-Level Verification

PROFESSIONAL EXPERIENCE

- **Senior Hardware Engineer, Otter Creek Electronics, Brattleboro, VT**
2023 – Present
 - Achieved a 96.7% hardware validation pass rate across 4 FPGA-based control boards by standardizing simulation and board-level test sequences and reviewing interface specifications with design staff.
 - Accelerated the embedded sensor project timeline by 37 days by parallelizing VHDL synthesis and board-level verification tasks with the layout team.
 - Reduced security vulnerabilities by 29.3% on a network gateway module by applying cybersecurity system hardening requirements and patching 7 firmware-level exploits.
 - Consulted specifications with cross-functional engineering staff to evaluate hardware-software interfaces, resolving 9 signal-timing conflicts before tape-out.
- **Hardware Engineer II, Saxtons River Technology Group, Springfield, VT**
2021 – 2023
 - Raised hardware validation pass rate from 91.2% to 95.8% on a power management board by adding boundary-scan tests and refining clock-domain crossing checks.
 - Shortened the motor-controller redesign timeline by 28 days by scripting automated regression tests in Python that ran overnight on 14 test vectors.
 - Provided technical support to marketing and sales departments during 3 product launches, translating board capabilities into customer-facing specification sheets.
 - Identified and mitigated 4 security vulnerabilities in a diagnostic interface by restricting debug port access per cybersecurity system hardening requirements.
- **Hardware Engineer I, West River Embedded Systems, Keene, NH**
2020 – 2021
 - Accelerated a mixed-signal prototype timeline by 18 days by completing schematic capture and layout review 2 weeks ahead of the original milestone.
 - Trained 6 system designers on digital oscilloscope measurement procedures and test documentation practices.

- Characterized RF filter performance using network analyzers, logging insertion-loss data across 312 frequency points to validate board-level compliance.